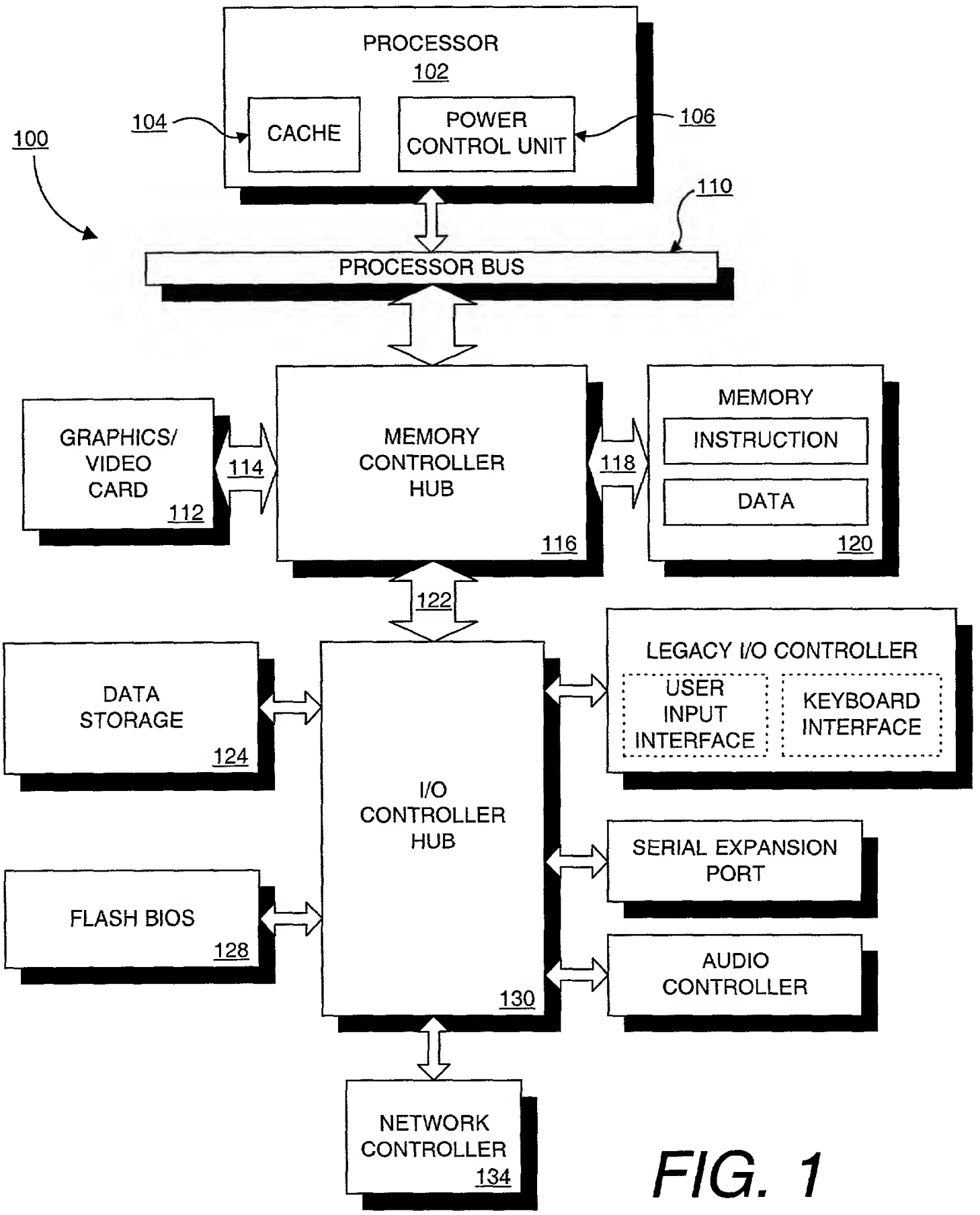

PROCESSOR
102
CACHE
104
POWER
CONTROL UNIT
106
100
110
PROCESSOR BUS
GRAPHICS/
VIDEO
CARD
112
114
MEMORY
CONTROLLER
HUB
116
118
MEMORY
INSTRUCTION
DATA
120
122
DATA
STORAGE
124
I/O
CONTROLLER
HUB
LEGACY I/O CONTROLLER
USER
INPUT
INTERFACE
KEYBOARD
INTERFACE
SERIAL EXPANSION
PORT
AUDIO
CONTROLLER
FLASH BIOS
128
130
NETWORK
CONTROLLER
134

FIG. 1

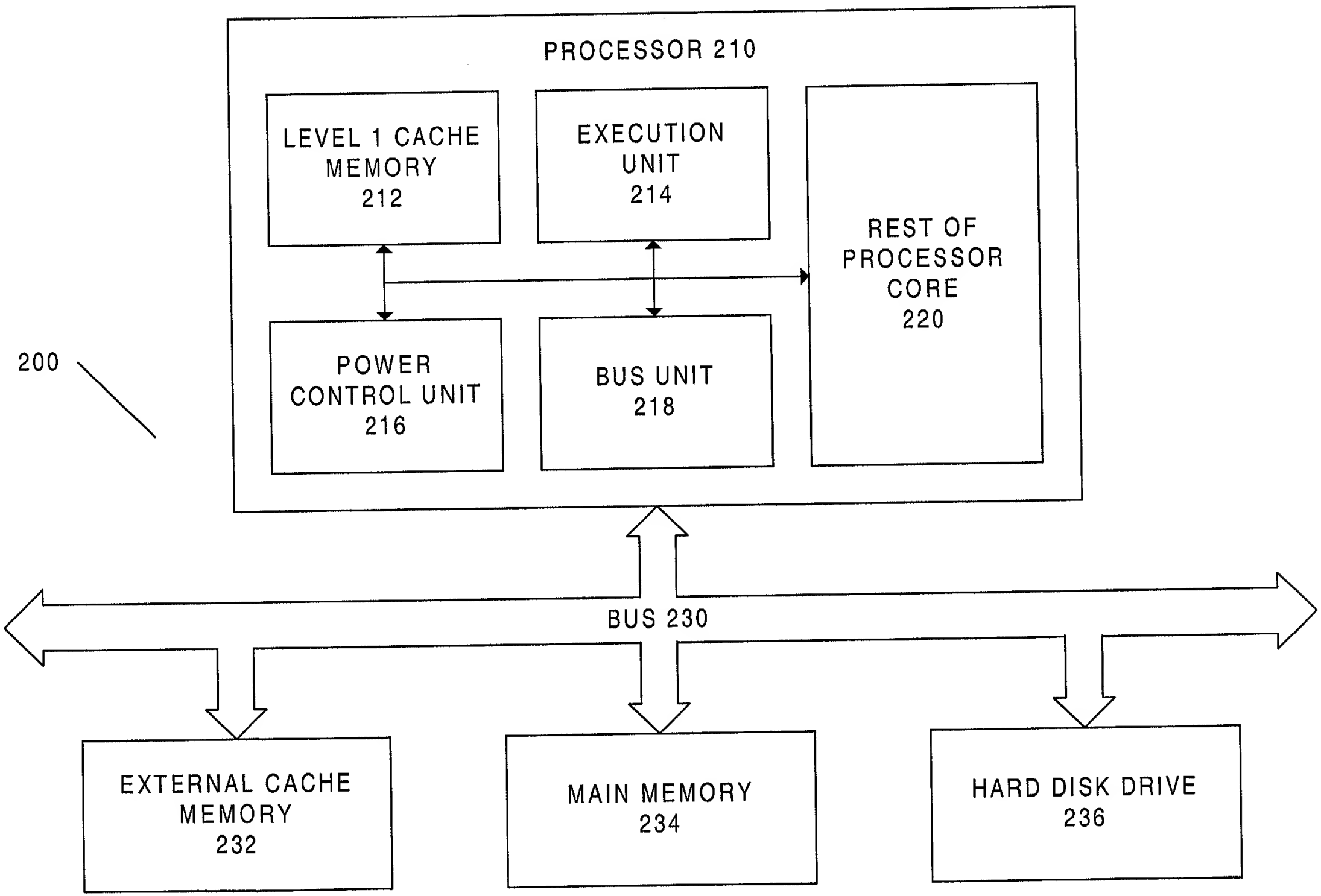

200
PROCESSOR 210
LEVEL 1 CACHE MEMORY 212
EXECUTION UNIT 214
REST OF PROCESSOR CORE 220
POWER CONTROL UNIT 216
BUS UNIT 218
BUS 230
EXTERNAL CACHE MEMORY 232
MAIN MEMORY 234
HARD DISK DRIVE 236

FIG. 2

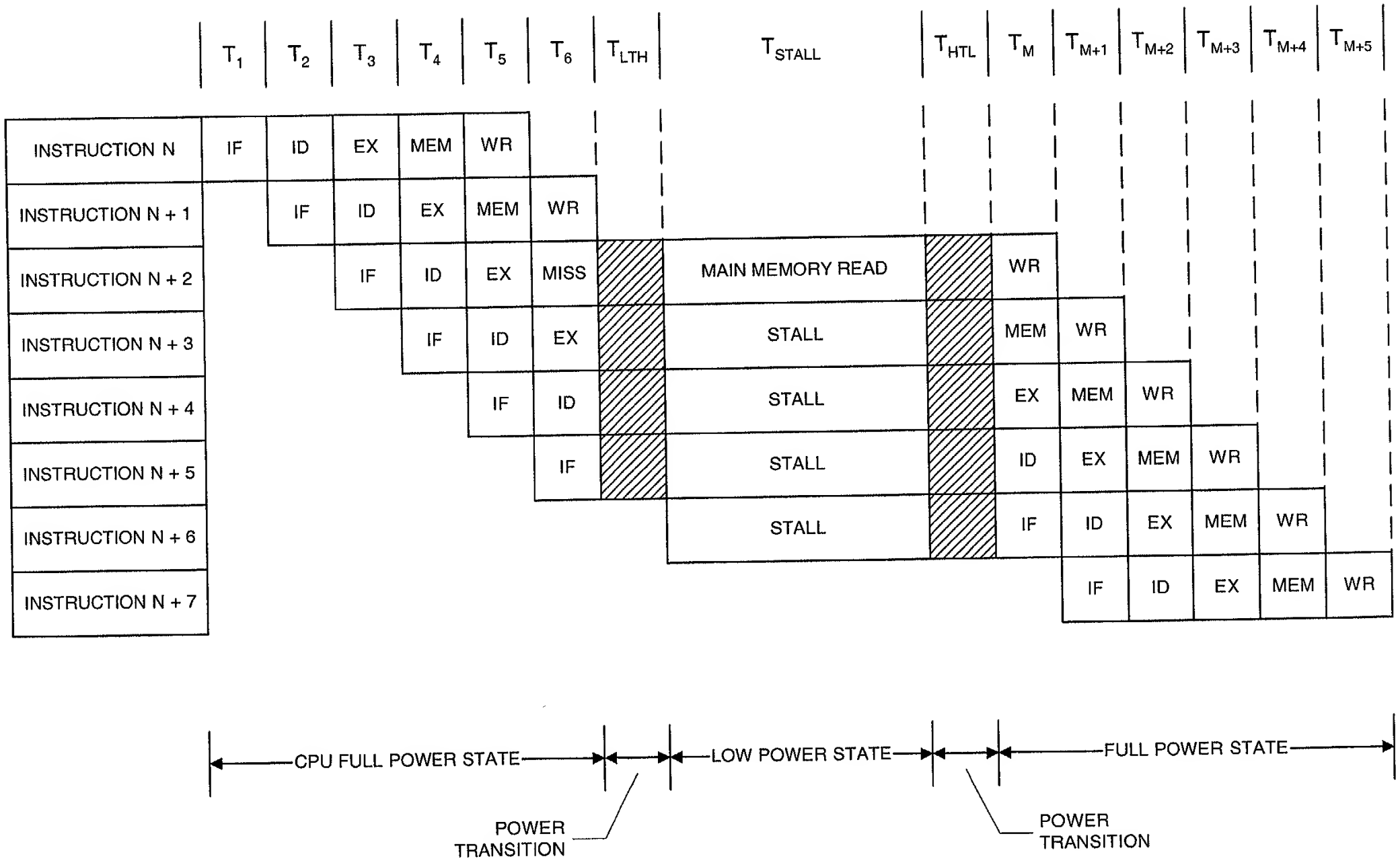
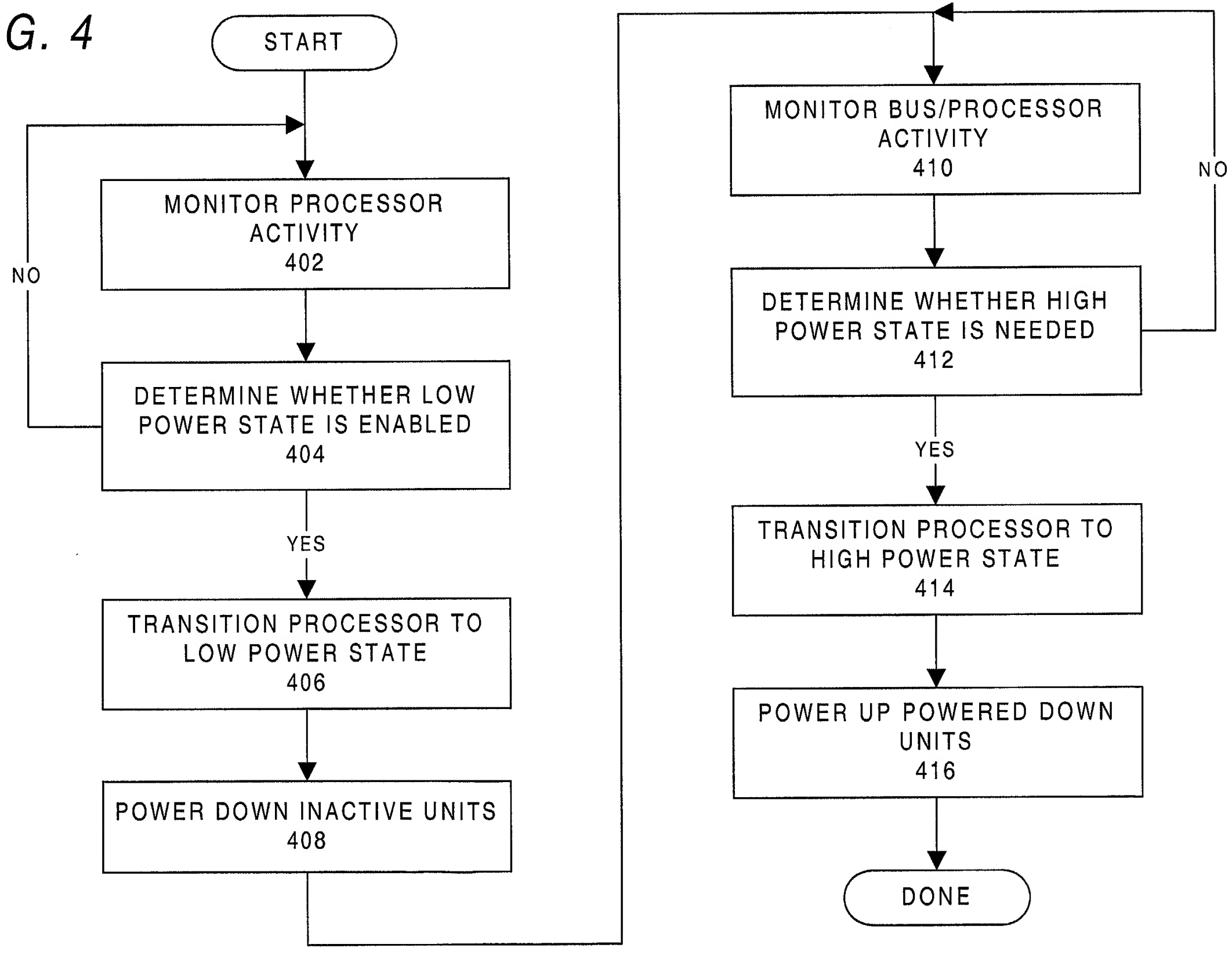

T1
T2
T3
T4
T5
T6
TLTH
TSTALL
THTL
TM
TM+1
TM+2
TM+3
TM+4
TM+5
INSTRUCTION N
INSTRUCTION N + 1
INSTRUCTION N + 2
INSTRUCTION N + 3
INSTRUCTION N + 4
INSTRUCTION N + 5
INSTRUCTION N + 6
INSTRUCTION N + 7
IF
ID
EX
MEM
WR
MISS
MAIN MEMORY READ
STALL
CPU FULL POWER STATE
LOW POWER STATE
FULL POWER STATE
POWER TRANSITION
POWER TRANSITION

FIG. 3

FIG. 4


START
MONITOR PROCESSOR ACTIVITY 402
NO
DETERMINE WHETHER LOW POWER STATE IS ENABLED 404
YES
TRANSITION PROCESSOR TO LOW POWER STATE 406
POWER DOWN INACTIVE UNITS 408
MONITOR BUS/PROCESSOR ACTIVITY 410
DETERMINE WHETHER HIGH POWER STATE IS NEEDED 412
NO
YES
TRANSITION PROCESSOR TO HIGH POWER STATE 414
POWER UP POWERED DOWN UNITS 416
DONE